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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,145	02/28/2002	Andrew Mark Nightingale	550-310	5033

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EXAMINER	
LE, TOAN M	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,145	NIGHTINGALE, ANDREW MARK	
	Examiner	Art Unit	
	Toan M Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claims 3, 4, and 6 are objected to because of the following informalities:

Referring to claims 3, 4, and 6, line 1, "wherein said step (d)", there is no indication of step (d) being labeled in the claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by "The CoreConnect Bus Architecture", IBM (Referred hereafter IBM).

Referring to claims 1, and 16-17, IBM discloses a method, a computer program and a carrier medium operable to configure a processing unit to perform a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, the method comprising the steps of:

(a) reading a configuration file containing predetermined parameters identifying the type of the device and capabilities of the device (page 7, DCR Bus section: lines 1-2);

(b) employing a configuration engine to dynamically generate a test environment for the device by creating selected test components which are coupled via the bus with a

representation of the device to form the test environment, the test components being selected dependent on the configuration file (page 7, Design Toolkits section: 1st and 2nd paragraphs);

causing a test sequence to be executed (page 7, Design Toolkits section: 2nd paragraph); and

monitoring signals passed between the representation of the device and one or more of the test components during execution of the test sequence to generate result data indicating compliance with the bus protocol (page 7, Design Toolkits section: 3rd paragraph).

As to claim 2, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, wherein the configuration file is selected from a set of configuration file templates, the set containing a configuration file template for each type of device, and each configuration file having a number of entries for providing configuration information specific to the device (page 7, Design Toolkits section: lines 7-8).

Referring to claim 3, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, comprises the step of employing a protocol checking component to check that signals passed between the representation of the device and one or more of the test components during execution of the test sequence do not violate a set of predetermined rules of the bus protocol (page 7, Design Toolkits section: 3rd paragraph).

As to claim 4, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip comprises the step of employing a coverage monitoring component to

monitor signals passed between the representation of the device and one or more of the test components during execution of the test sequence to determine whether a set of coverage points are observed (page 7, Design Toolkits section: lines 11-14).

Referring to claim 5, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, wherein the set of coverage points is configured dependent on the configuration file read at the step (a) (page 7, Design Toolkits section: lines 15-16).

As to claim 6, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip comprises the step of employing a protocol checking component to check that signals passed between the representation of the device and one or more of the test components during execution of the test sequence do not violate a set of predetermined rules of the bus protocol, and wherein, if all coverage points in the set have been observed without violating any of the set of predetermined rules of the bus protocol, the method further comprises the step of generating an output confirming compliance with the bus protocol (page 7, Design Toolkits section: lines 12-14).

Referring to claim 7, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, wherein at the step (b) the step of creating selected test components comprises selecting the test components to be created in dependence on the type of device to be tested (page 7, Design Toolkits section: lines 7-8).

As to claim 8, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, wherein at least one of the test components has associated therewith a plurality of behaviors that it may exhibit, the choice of behavior being determined when that test component is created dependent on the type of device to be tested (page 7, Design Toolkits section: lines 8-10).

Referring to claim 9, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, wherein the test sequence is a user-definable test sequence developed for the device to be tested (page 7, Design Toolkits section: line 8).

As to claim 13, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, wherein the type of device that may be tested comprises a master, a slave, an arbiter or a decoder (figures 5-6).

Referring to claim 15, IBM discloses a method of testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, wherein the representation of the device is a Registration Transfer Language (RTL) representation (page 7, Design Toolkits section: 2nd paragraph).

As to claim 18, IBM discloses a data processing apparatus for testing compliance of a device with a bus protocol of a bus, the device being a component of a system-on-chip, and the bus being provided within the system-on-chip, the apparatus comprising:

memory for storing a configuration file containing predetermined parameters identifying the type of the device and capabilities of the device (page 3, lines 13-14); and

a processing unit (page 3, 2nd and 3rd paragraphs; figure 2) arranged to perform the steps of:

(i) dynamically generating a test environment for the device by creating selected test components which are coupled via the bus with a representation of the device to form the test environment, the test components being selected dependent on the configuration file (page 7, Design Toolkits section: 1st and 2nd paragraphs);

executing a test sequence (page 7, Design Toolkits section: 2nd paragraph); and

monitoring signals passed between the representation of the device and one or more of the test components during execution of the test sequence to generate result data indicating compliance with the bus protocol (page 7, Design Toolkits section: 3rd paragraph).

Claims 10-12 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for allowance of the claims 10-12 and 14 is generating the test environment including mapping signals within the interface module to signals within the test environment defined within the configuration file to identify a level of hierarchy of the representation of the device within the interface module to facilitate the mapping of signals and a trickbox component compatible with the bus protocol, which is the ARM AMBA bus protocol, to provide input/output interface.

Remarks

Response to Arguments

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

June 29, 2004

John Barlow
Supervisory Patent Examiner
Technology Center 2800